National Semiconductor

July 9, 2008

LM3678 High-Performance, Miniature 1.5A Step-Down DC-DC Converter for Handheld Applications

General Description

The LM3678 step-down DC-DC converter is optimized for powering low voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.5V to 5.5V. It provides up to 1.5A load current, over the entire input voltage range. LM3678 offers a 0.8V/1.2V option. One of the pair of voltages is set through the VSELECT pin.

LM3678 operates in PWM mode with a fixed frequency of 3.3MHz. Internal synchronous rectification provides high efficiency during PWM mode operation. In shutdown mode, the device turns off and reduces battery consumption to 0.01µA (typ).

The LM3678 is available in a 3mm x 3mm LLP-10 package. A high switching frequency of 3.3MHz (typ.) allows use of tiny surface-mount components. Only three external surface-mount components, an inductor and two ceramic capacitors, are required (solution size less than 33 mm^2). For voltages other than the voltage shown, please refer to ordering information section or **contact National Semiconductor**.

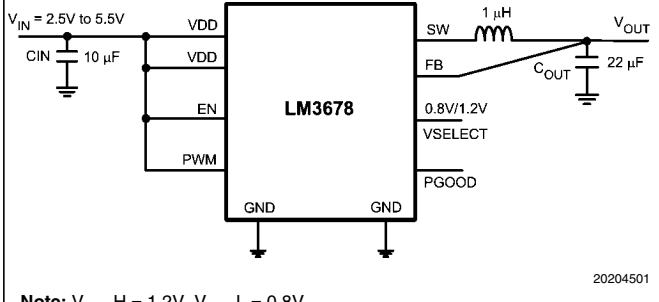
Features

- V_{OUT} = 0.8V/1.2V
- V_{IN} = 2.5V to 5.5V
- 1.5A maximum load capability
- 3.3MHz PWM fixed switching frequency (typ.) allows the use of 1µH inductor
- +/- 3% DC output voltage precision
- 0.01µA typical shutdown current
- Internal synchronous rectification for high efficiency
- Internal soft start
- Current overload and thermal shutdown protection

Applications

- PDAs and Smart Phones
- Personal Media Players
- W-LAN
- USB Modem Applications
- Digital still cameras
- Portable Hard disk drives

Typical Application Circuit



Note: V_{SEL} H = 1.2V, V_{SEL} L = 0.8V

Efficiency vs. Output Current (V_{OUT} = 1.2V)

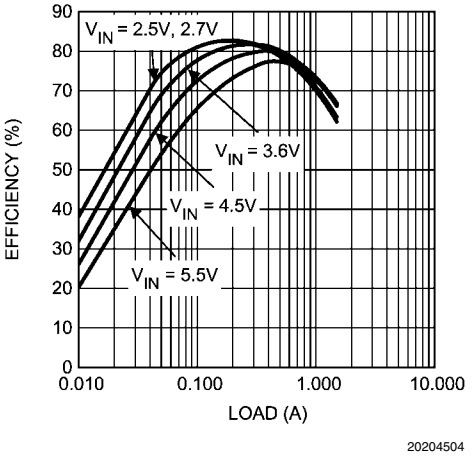


FIGURE 1.

Functional Block Diagram

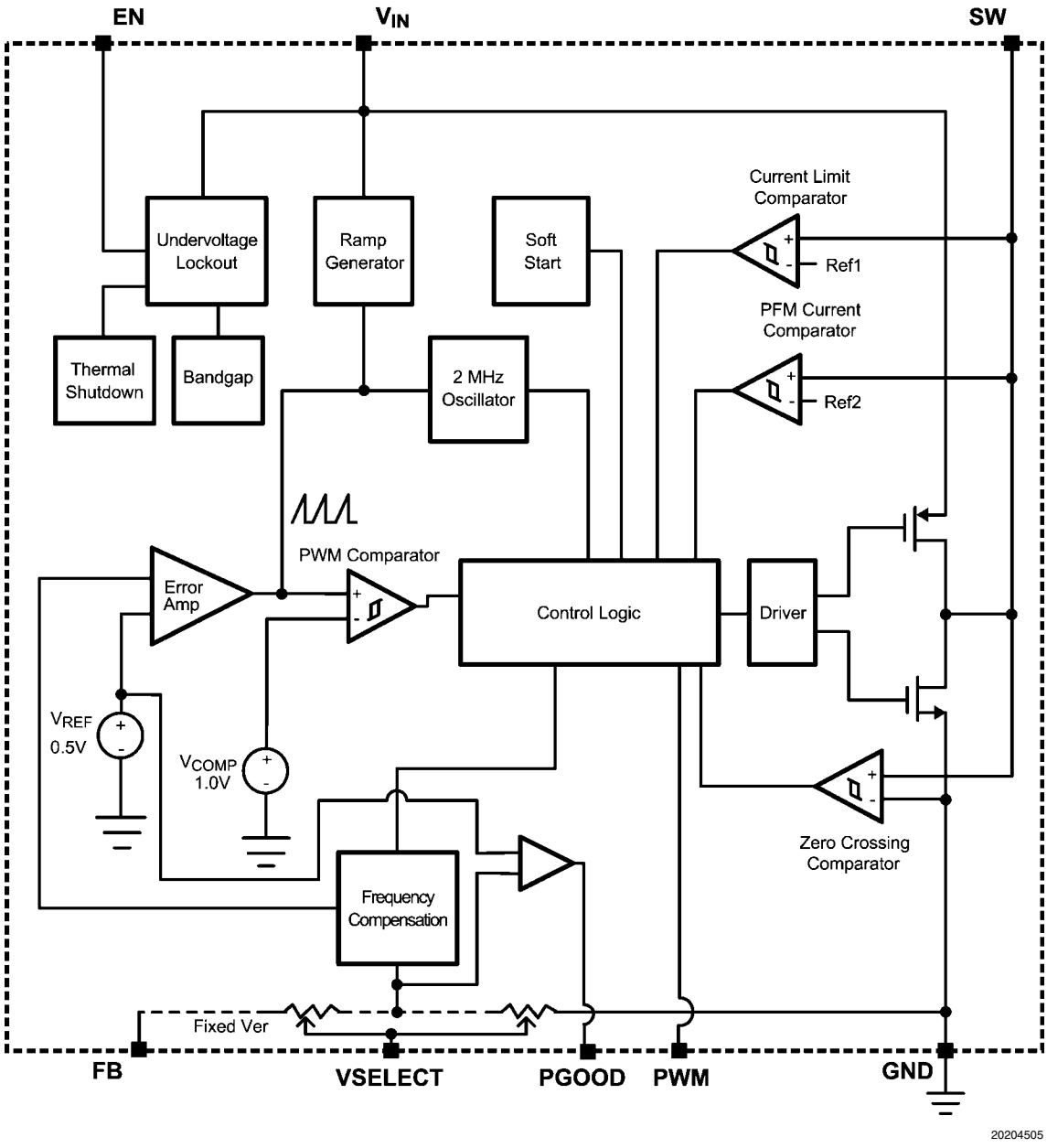
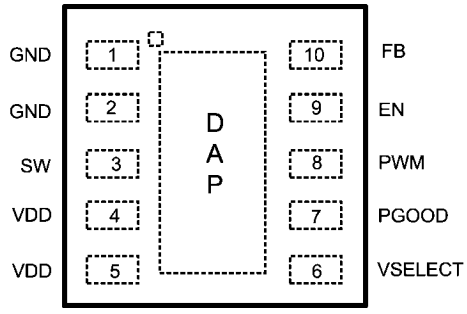
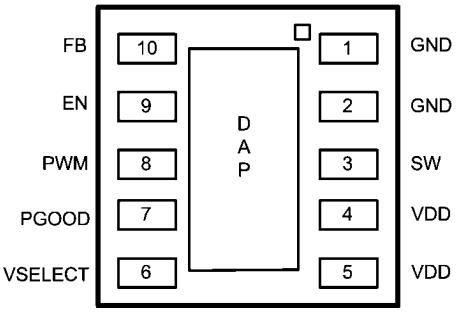


FIGURE 2. LM3678 Block Diagram

Connection Diagram and Package Mark Information



Top View



Bottom View

Pin Descriptions

Pin #	Name	Description
1	GND	Power Ground pin.
2	GND	Analog Ground Pin
3	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier
4	VDD	Analog supply input. Connect to the input filter capacitor (Figure 1).
5	VDD	Power supply Input. Connect to the input filter capacitor (Figure 1).
6	VSELECT	Output voltage select (For example) VSELECT = LOW, V_{OUT} = 0.8V VSELECT = HIGH , V_{OUT} = 1.2V
7	PGOOD	Power Good Flag. This commom drain logic output is pulled to ground when the output voltage is not within +/-7.5% of regulation.
8	PWM	Connect PWM pin to VIN.
9	EN	Enable pin. The device is in shutdown mode when voltage to this pin is <0.4V and enabled when >1.0V. Do not leave this pin floating.
10	FB	Feedback analog input. Connect directly to the output filter capacitor for fixed voltage versions.
DAP	DAP	Die Attach Pad, connect the DAP to GND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

Ordering Information

Voltage Option	Order Number	Package Marking	Supplied As
0.8V/1.2V	LM3678SDE-1.2	S021B	250 units, Tape-and-Reel
	LM3678SD-1.2	S021B	1000 units, Tape-and-Reel
	LM3678SDX-1.2	S021B	4500 units, Tape-and-Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} Pin: Voltage to GND	−0.2V to 6.0V
EN Pin:	−0.2V to 6.0V
FB, SW Pin:	(GND−0.2V) to (V_{IN} + 0.2V)
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)	260°C

Operating Ratings (Notes 1, 2)

Input Voltage Range	2.5V to 5.5V
Recommended Load Current	0mA to 1.5A
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (Note 4)	−30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (LLP-10) for 4 layer board (Note 5)	49.8°C/W

Electrical Characteristics (Notes 2, 6, 8)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to the LM3678 Typical Application Circuit (pg. 1) with V_{IN} = EN = 3.6V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	VSELECT = Low & High	**-3**		**+3**	%
V_{REF}	Internal Reference Voltage	(Note 7)		0.5		V
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN}= V_{GS}= 3.6V		150	**200**	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET	V_{IN}= V_{GS}= 3.6V		110	**150**	mΩ
I_{LIM}	Switch Peak Current Limit	Open loop	**1.9**	2.15	**2.4**	A
I_{SHDN}	Shutdown Supply Current	EN = 0V			1	µA
EN_{IH}	Logic High Input	V_{IN} = 3.6V	**1.2**			V
EN_{IL}	Logic Low Input	V_{IN} = 3.6V			**0.4**	V
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**2.7**	3.3	**3.6**	MHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150°C (typ.) and disengages at T_J= 130°C (typ.).

Note 4: In Applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation: T_{A-MAX}= T_{J-MAX} − (θ_{JA}x P_{D-MAX}).

Note 5: Junction to ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

Note 6: Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

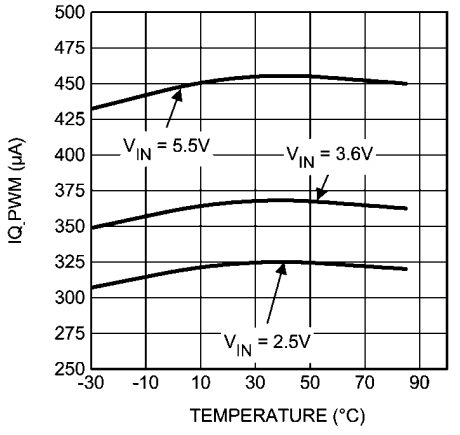
Note 7: Min and Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: The parameters in the electrical characteristic table are tested at V_{IN}= 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.

Typical Performance Characteristics

LM3678SD, Circuit of *Figure 1*, V_{IN}= 3.6V, V_{OUT}= 1.2V, C_{IN} = 10µF, C_{OUT} = 22µF, and T_A= 25°C, unless otherwise noted.

Quiescent Supply Current vs. Temperature



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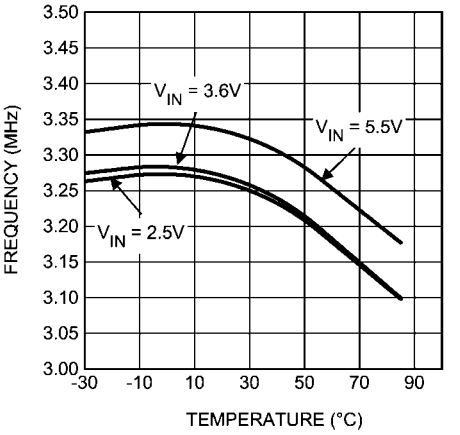
Switching Frequency vs. Temperature



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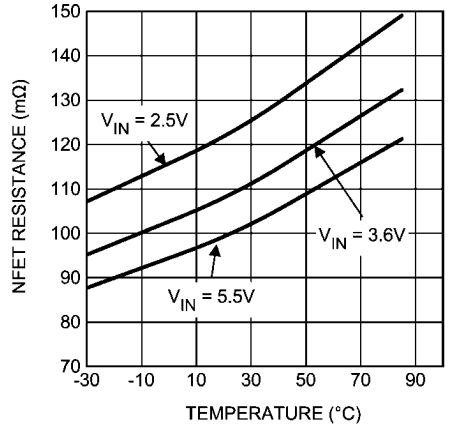
NFET_ R_{DSON} vs. Temperature



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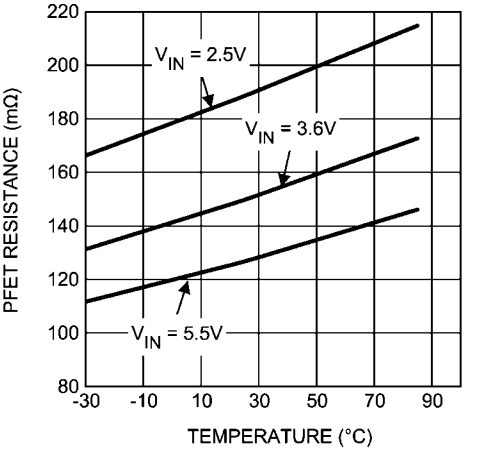
PFET_R_{DSON} vs. Temperature



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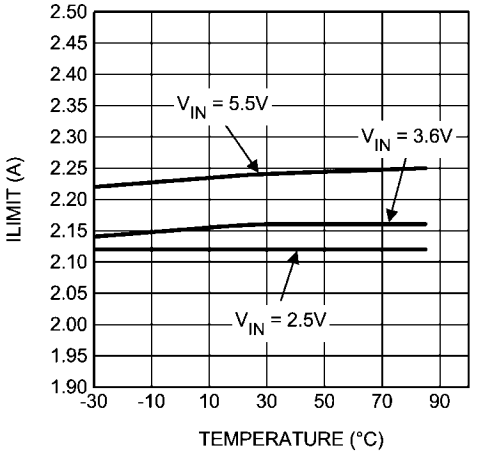
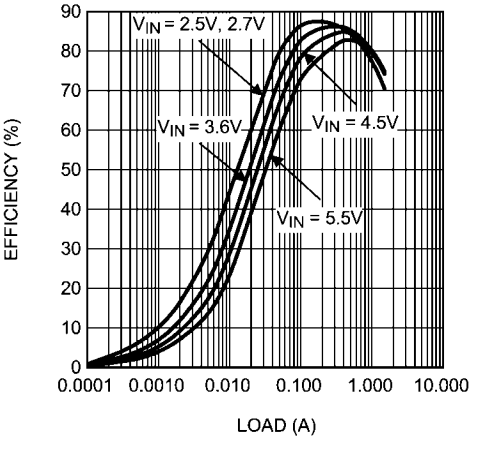
ILIMIT vs. Temperature (Open Loop)



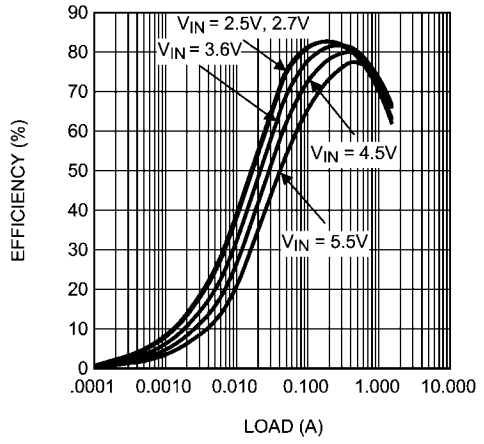
20204538

Efficiency PWM Mode vs. ILOAD (0.8V)



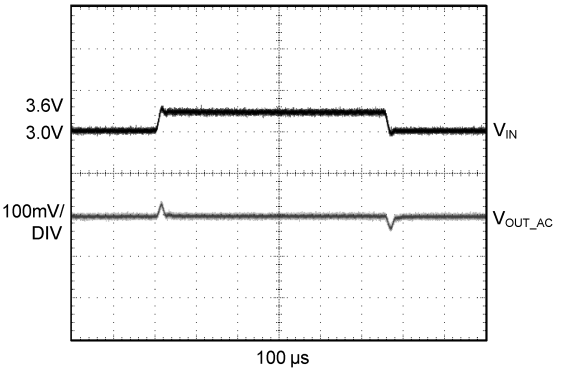
20204522

Efficiency PWM Mode vs. ILOAD (1.2V)



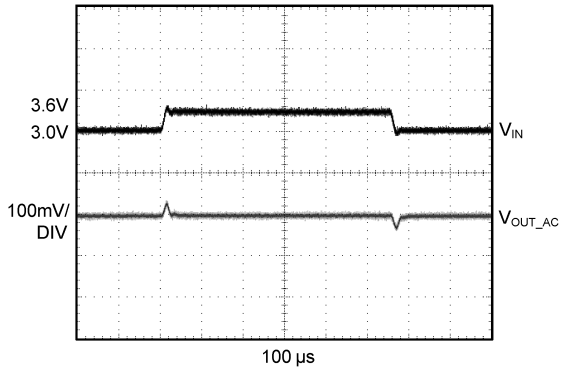
20204523

Line Transient Response
(V_{OUT} = 0.8V, LOAD = 500mA)



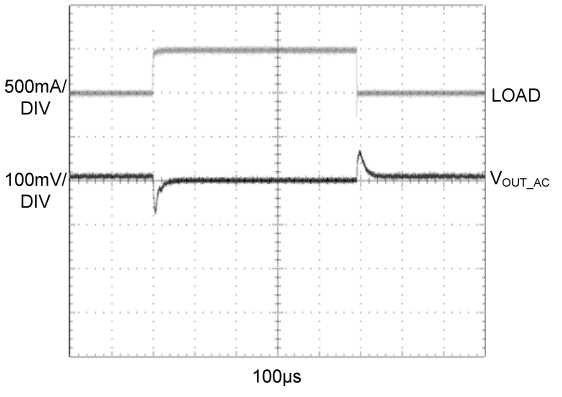
20204552

Line Transient Response
(V_{OUT} = 1.2V, LOAD = 500mA)



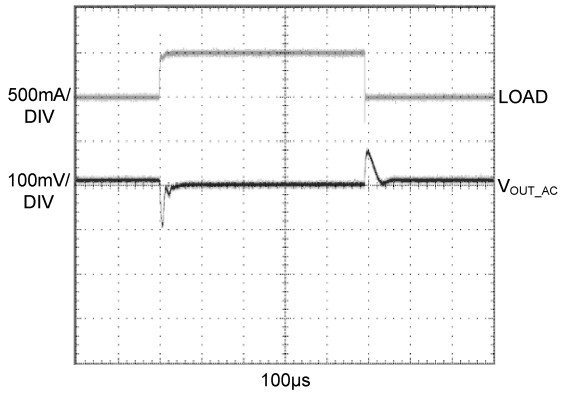
20204553

Load Transient Response
(V_{IN} = 3.6V, V_{OUT} = 1.2V, Load Step 0 ↔ 500mA)



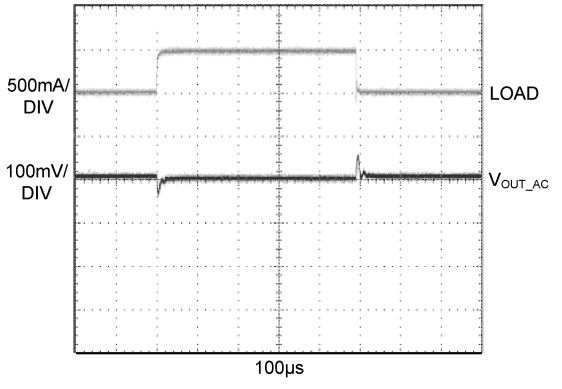
20204513

Load Transient Response
(V_{IN} = 3.6V, V_{OUT} = 0.8V, Load Step 0 ↔ 500mA)



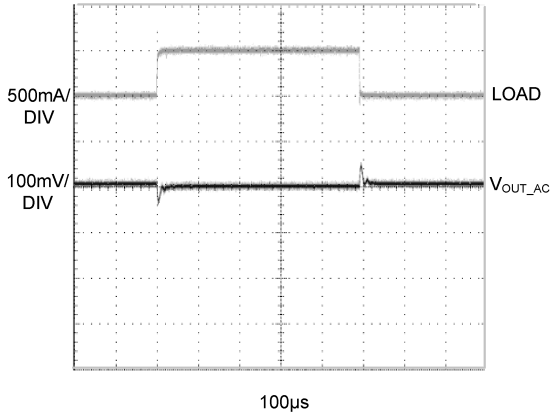
20204514

Load Transient Response
(V_{IN} = 3.6V, V_{OUT} = 0.8V, Load Step 500mA ↔ 1A)



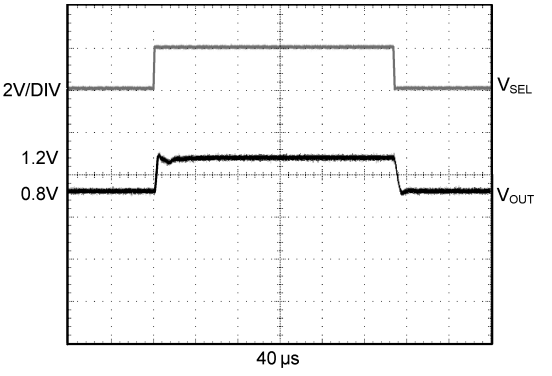
20204515

Load Transient Response
(V_{IN} = 3.6V, V_{OUT} = 1.2V, Load Step 500mA ↔ 1A)



20204520

VSELECT Transient Response
(V_{IN} = 3.6V, LOAD = 500mA)



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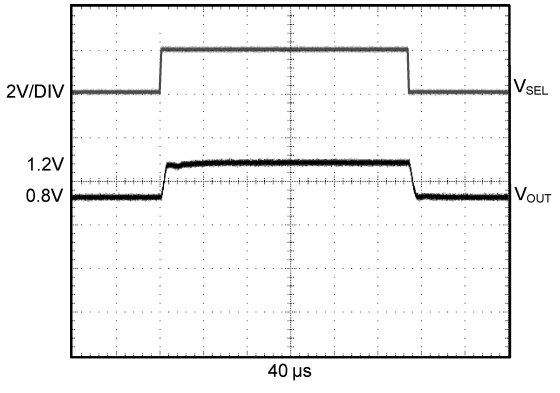
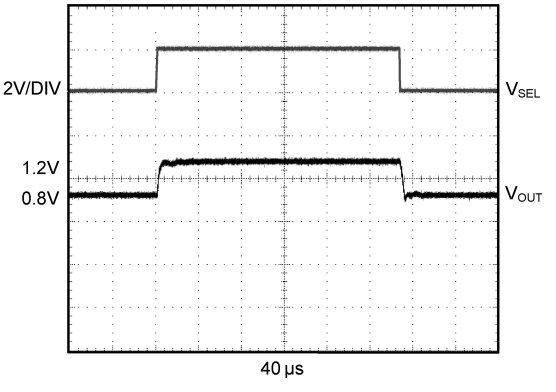
VSELECT Transient Response
(V_{IN} = 3.6V, No LOAD)



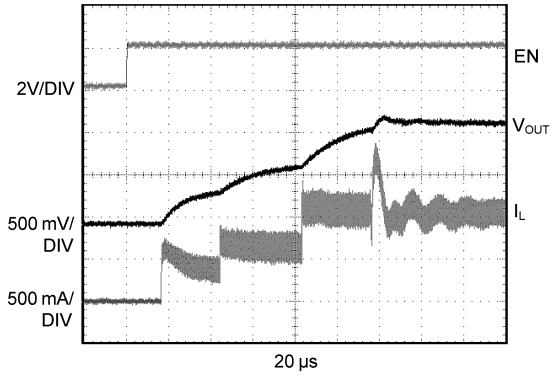
20204542

VSELECT Transient Response
(V_{IN} = 3.6V, LOAD = 1A)



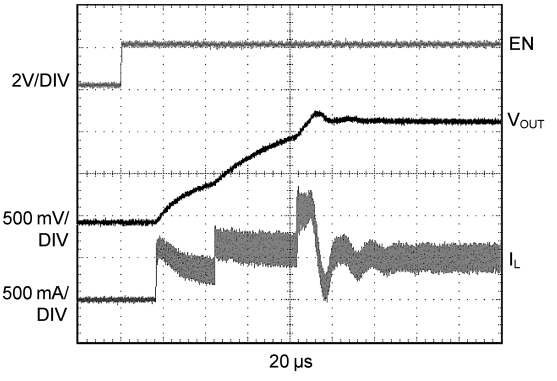
20204547

Start Up
(V_{IN} = 3.6V, V_{OUT} = 1.2V, LOAD = 1A)



20204550

Start Up
(V_{IN} = 3.6V, V_{OUT} = 1.2V, LOAD = 500mA)



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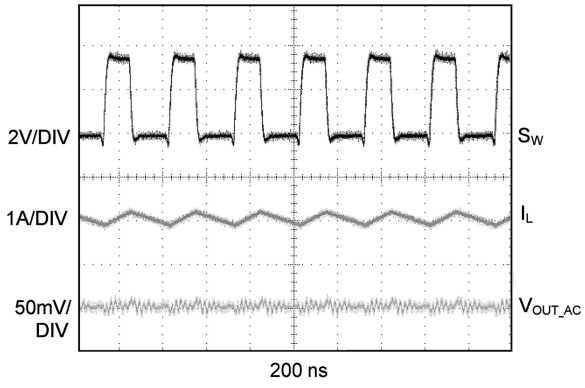
Switching Waveform
(V_{OUT} = 1.2V, LOAD = 1A)



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Operation Description

DEVICE INFORMATION

The LM3678, a high efficiency step down DC-DC switching buck converter, delivers a constant voltage from a single Li-Ion battery and input voltage rails from 2.5V to 5.5V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3678 has the ability to deliver up to 1.5A depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in *Figure 1*, only three external power components are required for implementation.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.5V or higher.

CIRCUIT OPERATION

During the first portion of each switching cycle, the control block in the LM3678 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN}–V_{OUT})/L$, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of - V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During device operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

The output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

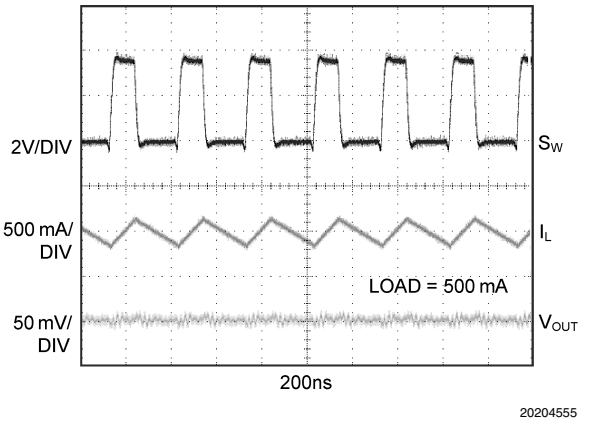


FIGURE 3. Typical PWM Operation

INTERNAL SYNCHRONOUS RECTIFICATION

The LM3678 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows the LM3678 to protect itself and external components during overload conditions by implementing current limiting with an internal comparator that trips at 2.15A (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay, thereby preventing runaway.

SHUTDOWN MODE

Setting the EN input pin low (<0.4V) places the LM3678 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3678 are turned off. Setting EN high (>1.0V) enables normal operation. It is recommended to set EN pin low to turn off the LM3678 during system power up and undervoltage conditions when the supply is less than 2.5V. Do not leave the EN pin floating.

SOFT START

The LM3678 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.5V. Soft start is implemented by increasing switch current limit in steps of 250mA, 500mA, 1A and 2A (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up.

Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and should be preferred.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average to peak inductor current
- I_{OUTMAX}: maximum load current (1.5A)
- V_{IN}: maximum input voltage in application
- L : minimum inductor value including worst case tolerances (30% drop can be considered for method 1)
- f : minimum switching frequency (2.7Mhz)
- V_{OUT}: output voltage

For a more conservative approach, a 1µH inductor with a saturation current rating of at least 2.5A is recommended for most applications.

Input Capacitor Selection

A ceramic input capacitor of 10uF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the LM3678 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$

TABLE 1. Suggest Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (max)	I_{SAT}
NR4012T1R0N	Taiyo Yuden	4 x 4 x 1.2	60mΩ	2.5A
LPS4012-102L	Coilcraft	3.9 x 3.9 x 1.2	100mΩ	2.5A
LPS4012-102L	Coilcraft	3.9 x 3.9 x 1.8	40mΩ	3.4A

Output Capacitor Selection

A ceramic output capacitor of 22µF, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follow:

$$V_{PP-C} = \frac{I_{RIPPLE}}{4 * f * C}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follow:

$V_{PP-ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase the rms (root mean squared) value can be used to get an approximate value of peak-to-peak ripple.

The peak-to-peak ripple voltage rms value can be expressed as follow:

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

TABLE 2. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
10µF for C_{IN}				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)
22µF for C_{OUT}				
JMK212BJ226MG	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

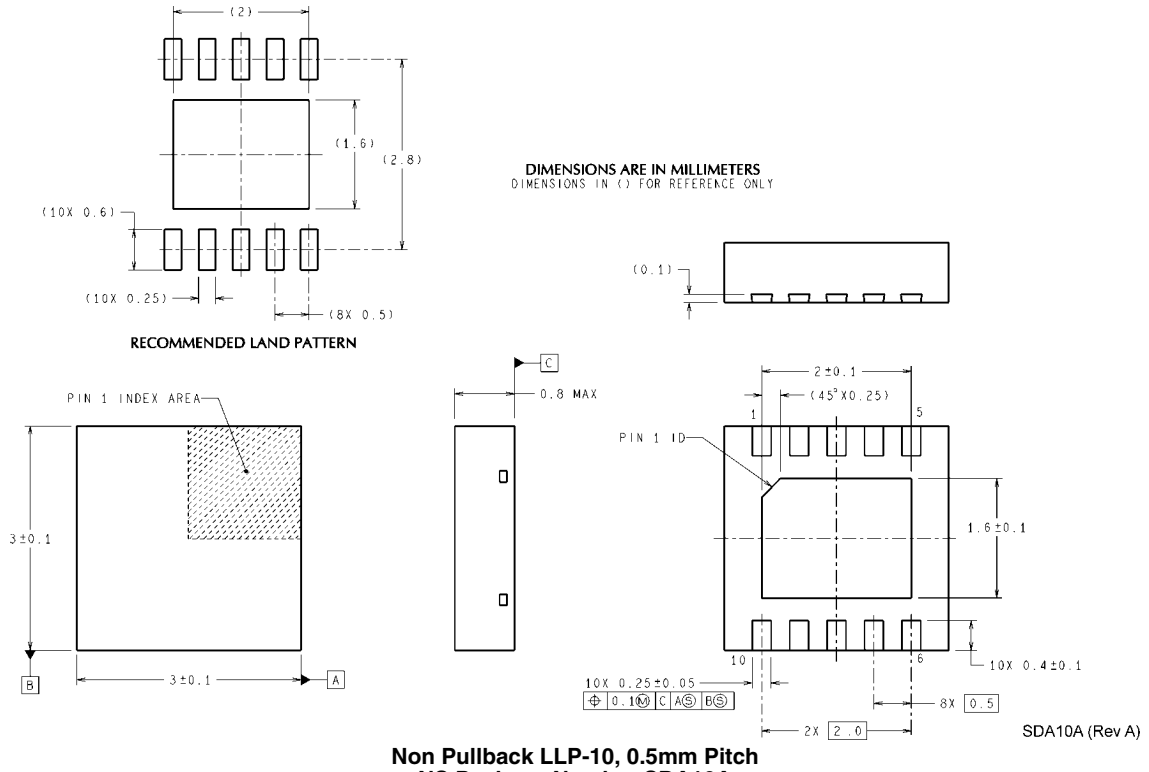
Good layout for the LM3678 can be implemented by following a few simple design rules below.

1. *Place the LM3678, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor through the LM3678 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3678 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LM3678 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3678 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3678 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

For detailed layout information, refer to Application Note 1722 *LM3678 Evaluation Board*.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

Physical Dimensions inches (millimeters) unless otherwise noted



Non Pullback LLP-10, 0.5mm Pitch
NS Package Number SDA10A
The dimensions for X1, X2, and X3 are as given:
X1 = 3mm +/- 0.030mm
X2 = 3mm +/- 0.030mm
X3 = 0.800mm +/- 0.075mm

Notes

Notes

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LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
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